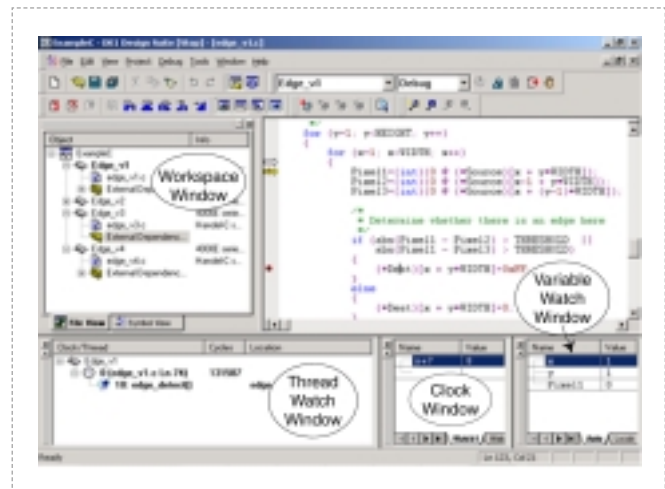


>: Celoxica DK1 Design Suite

Highlights

- Accelerates design cycle time with a direct flow from C-to-hardware for rapid prototyping and the development of first generation electronic products
- Empowers system architects and software engineers to design hardware, reducing the size of design teams required
- Produces predictable results from a language based on ISO/ANSI-C, extended with parallelism and control over timing
- Compresses design cycle time by enabling hardware and software design to occur in parallel via co-simulation
- Immediate productivity by integrating project management, simulation, synthesis and optimization



DK1's powerful GUI based project management and graphical debugger accelerate design cycle time by providing features that are familiar to both software engineers and system architects.

Product Overview

The Celoxica™ DK1 design suite is a unique C direct-to-hardware solution that enables application specialists to migrate concepts directly to hardware without requiring the generation, simulation, or synthesis of hardware description languages (HDLs). The DK1 design suite focuses on the design, validation, iterative refinement and implementation of complex algorithms in hardware. It includes built-in design entry, simulation, and synthesis, driven directly by Handel-C, a programming language based on ISO/ANSI-C. The output of the compiler is an architecture optimized EDIF netlist appropriate for FPGAs, or RTL VHDL for existing tool suites.

Because the design flow is streamlined, hardware can be designed in a fraction of the time and with a fraction of the team normally required. In addition, the Celoxica approach allows manufacturers to control resource issues by leveraging widely available software engineering skills at a new level within the design team.

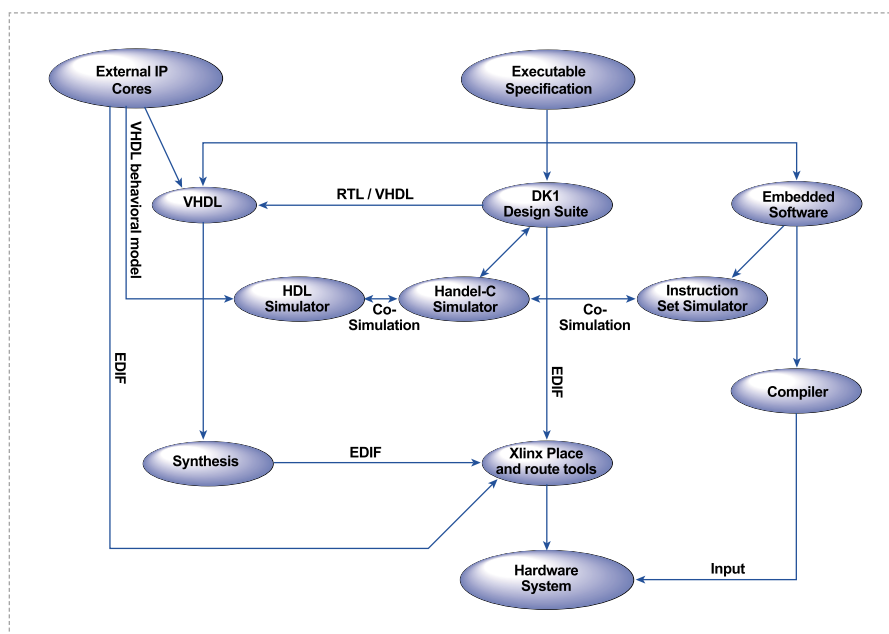
Empowers Software Developers

Unlike C-language approaches that try to extend C to look like an HDL, thus requiring hardware design expertise, the Handel-C and DK1 design suite have been created with system architects and software developers in mind. The Handel-C language has been designed to describe software algorithms which are subsequently compiled to hardware. DK1 includes functions typical of a software development environment, including a GUI for integrated project management, code editing and source level debugging.

Predictable Results

The Handel-C language is built around a very simple timing model. Assignments take exactly one clock cycle, giving the developer control of overall timing. Additional extensions include flexible data widths, parallel processing and communications between parallel elements. The model of parallelism is based on a sound mathematical formalism and therefore the resulting hardware design is deterministic.

In addition, the results of design changes are predictable, enabling iterative refinement of a design or engineering change orders (ECOs) late in the design cycle, with minimal impact on the schedule.



DK1's design flow enables design changes to be made with minimal impact on the design schedule. Changes in the Handel-C code produce predictable changes in hardware.

Superior Optimization Technology

The compiler generates architecture optimized EDIF netlists ready for input to FPGA place and route tools. This allows direct generation of prototype hardware, or first generation electronic products, in a fraction of the time when compared to traditional design methods.

Hardware/Software Co-Design

The built-in co-simulation feature facilitates co-design with instruction set simulators, VHDL simulators (such as ModelSim* from Model Technologies) and external C test benches. When used with DK1 this enables complete systems to be developed, thereby providing the ideal solution for board-level prototyping, reconfigurable SoC designs, and hybrid CPU + FPGA devices.

The co-simulation/co-verification design capability of the Celoxica DK1 design suite enables hardware/software partitioning decisions to occur much later in the design cycle. Existing C code from behavioral models can be converted quickly and simply into Handel-C. This facilitates the rapid development of software algorithms in C for conversion into hardware.

Product Features

Feature	Benefit
IDE for integrated project management, code editing and source level debugging	Typical of software development environment for ease-of-use by software developers
Built-in fast cycle-accurate simulator	Rapid, cycle-accurate, system-level verification
Integrated gate-level synthesis and optimization	No interim HDL stage, no additional code stream to maintain
Outputs architecture optimized EDIF	Drives FPGA place and route for Xilinx and Altera FPGAs
Optional RTL VHDL output	Drive traditional ASIC flow
Source level profiling of area and delay	Enables interactive optimization at the system level
Co-simulation of software, hardware and VHDL cores	Enables software and hardware design in parallel to compress design cycles
High-level language solution	Allows rapid development of FPGA designs and system-on-chip solutions
Based on ISO/ANSI-C	Allows application specialists to migrate concepts directly to hardware, for rapid prototyping and first generation electronic products
Language extensions to support flexible data widths, parallelism and communications	Very accessible to software engineers, predictable and controllable hardware behavior
Simple timing model	Easy to learn, simplifies interfacing to external hardware devices

System Requirements

The minimum system requirements to run DK1 is as follows:

- IBM PC compatible computer running Microsoft Windows 98/2000 or NT4.0
- Pentium II 233 MHz (or higher)
- 64Mb RAM, for systems running Windows 98, 128Mb RAM for NT4.0
- 40Mb of hard disk space
- CD-ROM drive
- Ethernet card (for software license)
- C compiler for simulation (Microsoft Visual C++ Ver.6.0 or greater, or GNU GCC 2.95.2 or greater)
- FPGA place and route tools to target FPGA hardware

In practice the amount of RAM required will depend on the size of compiled designs. The speed of the microprocessor will affect compilation and place and route times.

Recommended System Requirements

- IBM PC compatible computer running Microsoft Windows 98/2000 or NT4.0
- Pentium II, 450MHz (or higher)
- 256Mb of RAM
- 150Mb of hard disk space.
- CD-ROM drive.
- Ethernet card (for software license)
- C compiler for simulation (Microsoft Visual C++ Ver.6.0 or greater or GNU GCC 2.95.2 or greater)
- FPGA place and route tools to target FPGA hardware

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